光ネットワーク実現に向けたフォトニックパケットスイッチの技術課題

北山　研一*　　　　村田　正幸**

大阪大学

*大学院工学研究科

〒565-0871 大阪府吹田市山田丘 2-1

E-mail: kitayama@comm.eng.osaka-u.ac.jp

**サイバーメディアセンター

〒560-0043 大阪府豊中市

E-mail: murata@ics.es.osaka-u.ac.jp

あらまし MPλS の問題点を論じ、フォトニックパケットスイッチングをその究極のソリューションと位置付ける。次に光符号フォトニックラベルを用いたフォトニックパケットスイッチのアーキテクチャを提案し、その構成方法を述べる。最後に、そのスイッチングパーフォーマンスを明らかにする。

キーワード MPLS, MPλS, 光符号, フォトニックラベル, IP パケット, バッファ, ファイバ遅延線

Capability of Photonic Packet Switching

Ken-ichi Kitayama* and Masayuki Murata**

*Graduate School of Engineering, Osaka University

Suita, Osaka 567-0871, Japan

kitayama@comm.eng.osaka-u.ac.jp

**Cybermedia Center, Osaka University

Toyonaka, Osaka 560-0043, Japan

murata@ics.es.osaka-u.ac.jp

Abstract First, we will discuss the limitations and difficulties of MPλS, and we will address that the photonic packet switching will be an ultimate solution to solve the problems of MPλS. Next, we will focus on the OC-based photonic packet switching. The advantages of OC-based photonic packet switching include ultrafast photonic label processing capability, optical buffering using WDM fiber delay lines incorporating with ultrafast wavelength conversion. Finally, the switching performance of the proposed photonic packet switch will be presented.

Key words MPLS, MPλS, optical code, photonic label, IP packet, buffer, fiber delay line

1. INTRODUCTION

Recent progress of wavelength division multiplexing (WDM) technology has significantly increased the point-to-point link capacity, providing scalable bandwidth for rapidly growing internet traffic demands. However, the capacity increase tends to shift the network capacity bottleneck from the link to the node due to rather slow packet processing capability in electronic layer at the node.

One promising technique to alleviate the bottleneck is via circuit-switched MPL(ambda)S (multi-protocol lambda switching) or MPλS technology [1,2] (Fig.1). The MPLS performs destination-based forwarding decisions only at the edges by eliminating forwarding task at the core nodes. MPλS is an extension of MPLS concept, enabling traffic engineering by provisioning wavelength paths or optical paths to establish a logical topology over WDM link network [3]. It allows the cut-through of the traffic not to be terminated at the node, and this is powerful to alleviate the load of router at the node. However, MPλS still poses several limitations such as a coarse forwarding granularity, small label space etc..

Photonic packet switching might be an ultimate solution in the long run to overcome the above problems of MPλS. It has been extensively studied; for example, the European KEOPS project has shown a broadcast-and-select switch [4], where wavelength converters are used to perform space switching and delay selection. Packet contention at the output ports can be resolved by utilizing fiber delay lines. Another example is the WASPNET prototype [5] that uses currently available optical devices such as tunable wavelength converters, arrayed waveguide gratings (AWG), and fiber delay lines to resolve contention. However, these photonic packet switches still rely on relatively slow electronic header processing and hence can provide the line interface only up to the bit rate of 10Gb/s.

To overcome both the problems of circuit-switched MPλS and slow electronic header processing in conventional photonic packet switchings, optical code (OC)-based photonic packet switching has recently been proposed [6].

In this paper, first we will discuss the limitations and difficulties of MPλS, and we will address that the photonic packet switching will be an ultimate solution to solve the problems of MPλS. Next, we will focus on the OC-based photonic packet switching. The advantages of OC-based photonic packet switching include ultrafast photonic label processing capability, optical buffering using WDM fiber delay lines (FDLs) incorporating with ultrafast wavelength convertors. Finally, the switching performance of the proposed photonic packet switch will be presented.

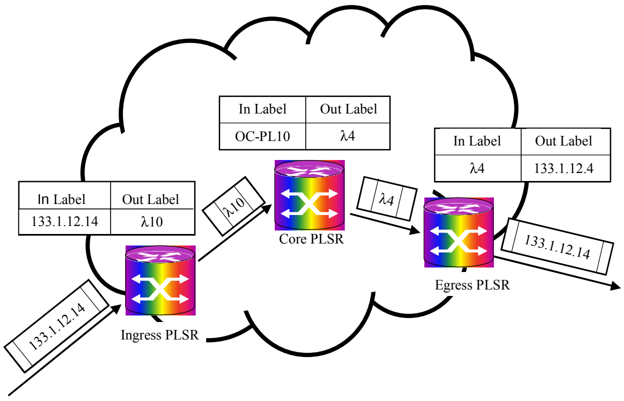

Fig1. MPλS network and its forwarding algorithm

2. WHY PACKET SWITCHING? AND WHY PHOTONIC ?

2.1 Limitations of MPλS

There have been pointed out some problems with MPλS [7]. A foremost difficult problem in MPλS is a capacity granularity; the unit of the bandwidth between edge node pairs of the MPLS domain is a wavelength capacity. It may be sometimes too large to accommodate the traffic between node pairs. Label (wavelength) merging and splitting in optical domain are fundamentally impossible in MPλS. The number of available wavelengths is too small for the label space to accommodate all the paths required (Table 1) as the wavelength resource is not abundant [8]. A few hundreds and even 1,000 wavelengths might be required as the labels for a nationwide backbone network [9].

Table 1 Photonic label space

	Number of codes	Label processings	Problems
Wavelength	Roughly 1000	Optical filtering	Difficulties in merge & split
Subcarrier	Roughly 100	RF filtering	Speed < 40Gb/s
Optical code	Abundant	Optical correlation	Impairments in transmission

Table.1

Another problem is how to establish the logical topology using optical paths suitable to deploying IP over WDM networks. The existing approaches impose that the traffic pattern is known a priori. This assumption is unrealistic because it is impossible to forecast the future traffic demand. The traffic load may be estimated by the traffic measurement. It implies that the traffic load can be known only after the network is established and operated. However, the existing approaches can determine the entire topology only after the traffic load is known. The bottleneck at the ingress and egress label switching routers (LSRs) is another problem in MPλS network. This is due to the traffic congestion as well as the insufficient capability of e-routers at the edges. One solution is to distribute packet processing, for example, by introducing WDM ring at the edge LSR [7]. However, we will end up with a demand for more powerful packet routers.

2.2 Limitaions of e-routers

In current e-router routers a bottleneck is caused by the longest prefix match for each incoming packet. The speed of a lookup algorithm of the routing table is determined by the number of memory accesses it requires to find the matching entry, and the speed of the memory access. The memory access time typically ranges from 10ns to 60ns. If an algorithm performs eight memory-lookups with a memory access time of 10ns, 12.5 million lookups/s can be performed [10]. The bit rate of the link interface with the router is, for example, only 10Gbps.

A physical size and electric power consumption of e-cross-connect (xc) switch and packet switch will become a severe problem in scaling up the switches as the network capacity grows. There is a forecast; if traffic volume continue to increase by a factor of four per year, which is the same rate as in U.S. in the year of 2000 [11], after two or three years the size of e-xc switch at 10Gbit/s becomes double or triple, and the e-packet switch at 10Gbit/s becomes larger than optical counterpart by a factor of 2 to 30. It is predicted that the e-power consumption of e-xc switch and e-packet switch will become lager by a factor of two to three, compared to optical switches regardless of the bit rate[12].

From the viewpoints of the processing capability of e-routers and the physical size and e-power consumption of e-XC switches, photonic technologies should be only an option to solve the above problems. In Table 2 the requirements which "*next-generation*" photonic packet switching has to achieve to meet demads for the future optical networkings are summarized. The packet processing over 1,000 times as powerful as e-router has might be requisite.

Table 2 Requirements for photonic packet switching

Performance	Target
Processing capability	1-100 [Gpps] 10-100 [Mpps]
Line bit rate	1-100 [Tbit/s] 10G [bit/s]
Number of address entries	1k-10k 10k-100k

Note 1 : Current electronic router
Note 2 : pps = Packet per second

Table.2

3. OPTICAL CODE-BASED PHTONIC PACKET SWITCHING

3.1 OC-photonic labels and the label processing

As shown in Fig.2, a basic idea of photonic packet switching is to encapsulate an IP packet into the *photonic wrapper*, which has a photonic label in the header as the identifier and perform forwarding using photonic labels.

The photonic label is simply a relatively short, fixed-length identifier that bears the information of either the label switched path (LSP) label. We will introduce OC-photonic label, in which each label is mapped onto an optical code, a sequence of optical pulses, so-called chip pulses [6]. The chip itself is a short pulse, and the time duration of the sequence has to be within a bit time duration. The number of optical code increases as the code length increases, and it could be abundant in practical applications, contrast to the scarcity of wavelength resource for the labels (Table 1). The number of optical codes increases further when the multi-level code such as QPSK code[13] is applied.

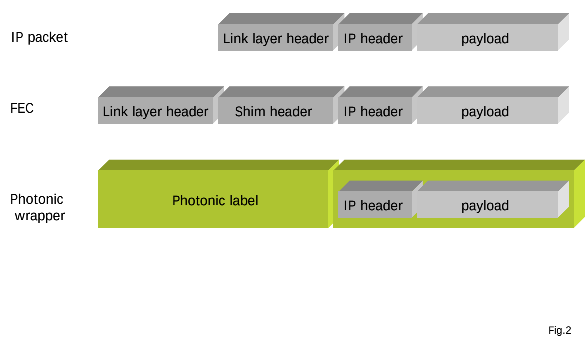

Fig.2 Concept of photonic wrapper with photonic label

The photonic label processor is structured with an optical correlator, a time-gate, optical thresholding, and an optical/electrical (O/E) conversion as shown in the block diagram in Fig.3. The time gate, which follows the optical correlator, allows only the auto-correlation mainlobe to pass by, rejecting the sidelobes. The OC-photonic label recognition is based upon the optical correlation between the optical codes. The optical correlation is performed by matched filtering in time domain. For example, a family of optical codes of 4-chip long codes and their auto-correlation waveforms are illustrated in Fig.4. The code is bipolar, in which the phase of optical carrier of individual chip pulse takes two states of either 0 or π. In the photonic label processing, the correlation output is time-gated, followed by the thresholding. Unique to the photonic label processing is that no optical logic operation is involved, and this is a key to the ultrahigh-speed operation of label processings.

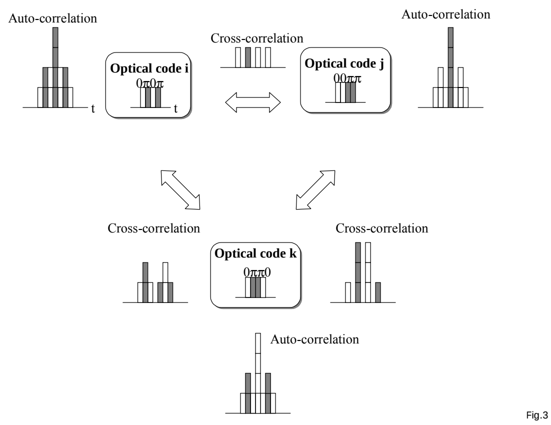

Fig.3 Photonic label processor

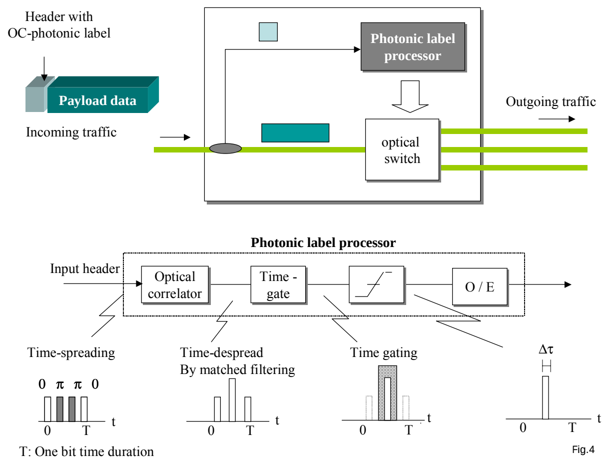

Fig.4 Optical correlation between two optical codes

There are several types of optical encoders; waveguide type of tapped delay line [6], fiber Bragg grating (FBG) [14], and holographic device [15]. The tapped delay line is a wave-guide device having an optical phase shifter on each arm, which is monolithically integrated on a silicon substrate. The FBG is a tiny optical fiber device, on which phase-shifted Bragg gratings are imprinted along the fiber axis. Both can generate bipolar optical codes. The optical encoder can be utilized for the optical correlator. The optical time gate has been achieved in an asynchronous system by using a semiconductor optical amplifier (SOA) based upon four-wave mixing (FWM)[6]. The gate width shorter than 10ps has been realized in the experiments. Very recently, an ultrafast optical thresholding has been demonstrated with fiber-optic nonlinear loop mirror [13]. Several high-speed off-the-shelf optical space switches have now become available.

3.2 Switch architecture

We have proposed an architecture of photonic packet switch with WDM-FDL buffering in Fig.5 [16]. It consists of three sections; optical switching unit, optical scheduling unit, and optical buffering unit. The wavelength converters indicated by supercontinuum light source with gate switches (SC + Gate) are added in the optical scheduling unit. The wavelength conversion allows incorporating WDM-FDL buffer [17] into the switch fabric. The WDM-FDL buffer virtually enhances the memory capacity by a factor of the number of wavelenghs W.

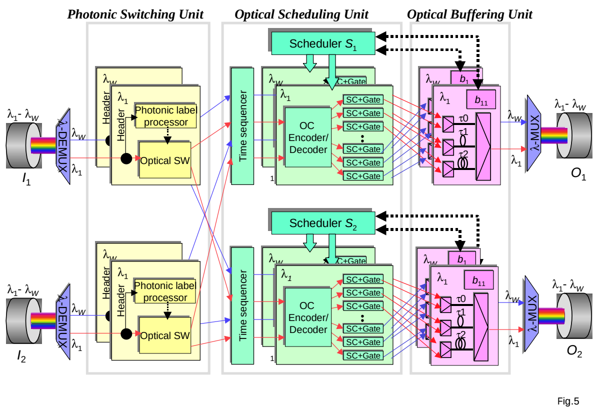

Fig.5 Architecture of photonic packet switch using WDM-FDL buffering

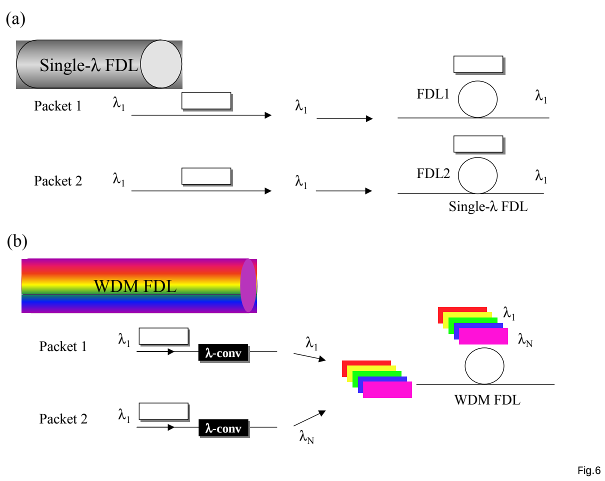

Fig.6 Fiber delay line buffer:Single λ vs. WDM

The photonic switching unit switches packets according to the packet header information. The header information is processed based upon the photonic label processing described in 3.1. If the packet is destined for the output port O_1, then the switch is set to the bar-state, directing the packet to the upper part of the optical switching unit.

The heart of our photonic switch is the optical scheduling unit. To schedule the packets destined for the output port O_i, the scheduler S_i of the output port O_i has to know the status of three delay lines τ_0, τ_1, and τ_2 with W different wavelengths. When the packet arrives, the scheduler searches the shortest queue. It can be easily determined by the counters b_{i1} through b_{iW}. A simple comparator in hardware may implement it. Once the wavelength for buffering is determined to be, say, λ_j, the scheduler updates the counter b_{ij} and sets the gate for tuning the wavelength. All incoming packets destined for the output port O_i should be processed in sequence. Let D be a delay line unit. Then, to delay the packet during iD, it is put on the i-th delay line (shown by τ_i in the figure). The counter b_{ij} keeps the buffer status information for wavelength λ_j going to the output port O_i. To handle the variable-length packets, it is incremented when the packet arrives at the optical buffer. It is decremented by one for every D time unit. Then, the next arriving packet is put on the b_{ij}-th delay line.

One problem is that we need to handle simultaneously arriving packets from different input ports. Each scheduler performs the above-mentioned operations for each packet exclusively for maintaining the valid counter, and it must not receive another packet during three-step operation. A time sequencer is introduced for this purpose. A role of the time sequencer is to delay another packet if the scheduler processes the packet. Since only a single packet arrives from an input port at a time, it is sufficient that a time sequencer is prepared for each input port.

4. SWITCHING PERFORMANCE

We will present the numerical results of performance of photonic packet switching. For more detail of the analysis, see [16]. In numerical examples, the packet arrival rate is set to be in proportion to the number of wavelengths W, and the traffic load per wavelength is fixed. For simple presentation, we set the average packet length to be unity, and set D to be relative to the average packet length.

The first result shows an effect of the delay line unit D in Fig.7. Six values of the number of wavelengths are considered: W = 1, 2, 3, 4, 6 and 8. The analytical results are plotted with solid lines. For W = 1, 2, 3 and 4, the simulation results are also presented to assess the accuracy of the analytic results. In simulation, we generated a billion packets. The traffic load ρ is fixed at 0.8 and the buffer depth B is set to be 64. From the figure, it is clear that the optimal value of D is around 0.3 irrespective of the number of wavelengths. Another observation is that the increasing number of wavelengths can dramatically improve the switch performance if D is appropriately selected. In the current example setting, the traffic load per wavelength is identically set. We confirmed that in the switch without wavelength conversion (W = 1) the packet loss probabilities are very high.

To clearly see the effect of introducing the wavelength conversion in the switch, we next plot the packet loss probabilities dependent on the number of wavelengths in Fig. 8. Five values of the traffic load are used: ρ = 0.65, 0.7, 0.75, 0.8 and 0.85. The buffer depth is set to be 64. The effect is apparent. Another view of the effect by the number of the wavelengths on is next presented for buffer dimensioning. Preparing the number B of delay lines for each output port directly affect the switch cost. Thus, the buffer size is an important design parameter. Figure 9 shows the packet loss probabilities dependent on B for W = 8, respectively. As can be observed in Fig.9, a quite large amount of the buffer is necessary to decrease the packet loss probabilities in the switch without wavelength conversion. By increasing the number of wavelengths W from 1 to 8, almost one-tenth of buffer capacity is sufficient to attain the same packet loss probabilities for given traffic load.

Finally, we discuss the optimization of the WDM buffer. There will be optimum values of the number of the wavelengths W and the number of delay lines, that is, the maximum buffer size B to satisfy a requirement for the packet loss probability. Let us set a criterion that the allowable packet loss probability is 10^{-9} for the traffic load ρ= 0.8. From the numerical simulations, for W = 1 and B > 800, and B decreases to 60 for W = 8. From another viewpoint, W > 13 for B = 64. By taking these results into consideration, it is concluded that the optimum range exists around W = 10 and B = 100. The buffer size of B = 100 corresponds to the fiber delay line length of 120m for the average packet size of 2,000 bits at the bit rate of 100Gb/s with D = 0.3. These numbers are practically feasible because WDM systems with more than 64 channels have already been commercialized, and the 120m-long optical fiber delay line could be constructed without using an optical fiber amplifier. It may be predicted that if WDM buffer has more than a few tens of wavelengths, the packet loss probability becomes almost negligible. This would be an ultimate goal of the WDM-FDL buffer.

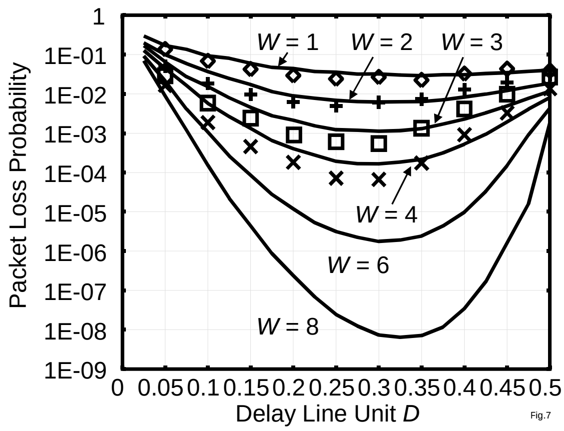

Fig.7 Packet loss probabilities dependent on D

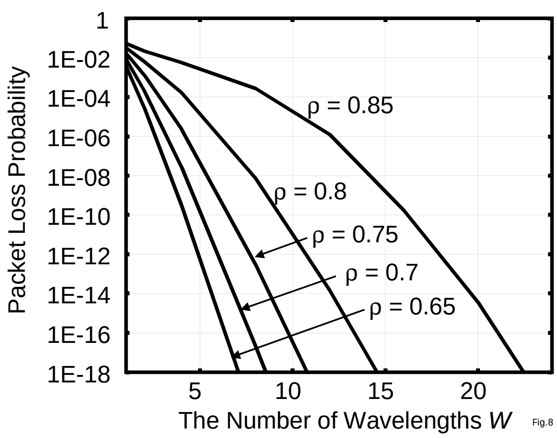

Fig.8 Packet loss probabilities depedent on the number of wavelengths W

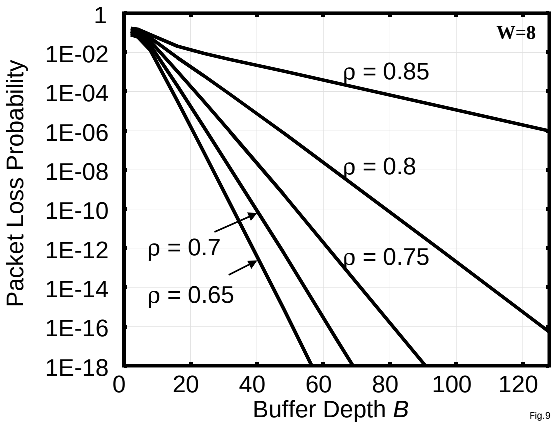

Fig. 9 Packet loss probabilities dependent on buffer depth *B* ($W = 8$)

5. CONCLUSION

We have discussed the limitations and difficulties of MPλS, and addressed that the photonic packet switching will be an ultimate solution to solve the problems of MPλS. Next, we have presented the OC-based photonic packet switching. The advantages of OC-based photonic packet switching include ultrafast photonic label processing capability, optical buffering using WDM –FDL incorporating with ultrafast wavelength conversion. Finally, the switching performance of the proposed photonic packet switch and its optimization have been presented.

References

[1] U. Black, *MPLS and Label Switching Networks*, Prentice Hall Inc., 2001.
[2] N. Ghani, "On IP-over-WDM Integration," *IEEE Communications Magazine*, pp.72-84, March 2000.
[3] D. O. Awduche, Y. Rekhter, J. Drake, and R. Coltun, "Multi-Protocol Lambda Switching: Combining MPLS Traffic Engineering Control with Optical Crossconnects," *IETF Internet Draft*, draft-awduche-mpls-te-optical-02.txt.
[4] A. Carena, M.D. Vaughn, R. Gaudino, M. Shell, and D.J. Blumenthal, "OPERA: An Optical Packet Experimental Routing Architecture with Label Switching Capacity," *J. Lightwave Technol.*, vol.16, pp.12135-2145, 1998.
[5] D. K. Hunter, et al., "WAPSNET: A wavelength switched packet network," *IEEE Communications Magazine*, pp.120-129, March 1999.
[6] K. Kitayama, N. Wada, and H. Sotobayashi, "Architectural Considerations of Photonic IP Router based upon Optical Code Correlation," *J. Lightwave Technol.*, vol.18, pp.183-1844, 2000.
[7] M. Murata and K. Kitayama, "A perspective on photonic multiprotocol label switching," *IEEE Network Magazine*., vol.15, pp.56-63, July/Aug. 2001.
[8] K. Sato and K. Kitayama, "Cutting-edge technologies on photonic backbone networks-Envisaged IP over photonic networks of the year of 2010(2)-," to appear in *IEICE*.
[9] K. Kitayama, M. Murata, and H. Miyahara, "A 1,000-ch. WDM network can resolve network bottleneck," Special Section on the *Asian-Pacific Conference on Communications (A PCC2001)* Proceedin*gs, .IEICE Trans. Commun*. vol.E84-B, p.113-116, 2001.
[10] S. Keshav and R. Sharma, "Issues and Trends in Router Design," *IEEE Communications Magazine*, pp.144-151, May 1998.
[11] L. G. Roberts and C. Crump, "U.S. Ip Internet traffic growth," *2001 CASPIAN NETWORKS, INC.*.
[12] S. Nojima, "Current status and the perspective of optical cross-connect," *Society Meeting of IEICE* (Sept. 2001).
[13] H. Sotobayashi, W. Chujo, and K. Kitayama, "1.6 bit/s/Hz, 6.4 Tbit/s OCDM/WDM (4 OCDM x 40 WDM x 40 Gbit/s) transmission," *27th European Conference on Optical Communications (ECOC2001),* PD.M.1.3 (Amsterdam 2001).
[14] M. C. Cardakli, D. Gurkan, S. A. Havstad, A. E. Willner, "Variable-bit-rate Header Recognition for Reconfigurable Networks using Tunable Fiber-Bragg-Gratings as Optical Correlators," *2000 Optical Fiber Conference (OFC2000)*, TuN2, (Baltimore, March 2000
[15] T. W. Mossberg and M. G. Rayner, *Optics&Photonics News*, pp.50-54, Match 2000.
[16] 村田, 北山, "非同期可変長パケットを扱うフォトニックラベルスイッチの提案,"*第１回ＰＮＩ研究会*(2001.7.13, 東京)
[17] L. Tancevski, A. Ge, G. Castanon, and L.S. Tamil, "A New Scheduling Algorithm for Asynchronous, Variable Length IP Traffic with Void Filling," *1999 Optical Fiber Conference (OFC '99)*, ThM7, (San Diego, Feb. 1999).